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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,833	07/20/2005	Robertus Theodorus Fransisc Van Schaijk	NL03 0024 US	9174

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EXAMINER	
PERT, EVAN T	
ART UNIT	**PAPER NUMBER**
2826	

NOTIFICATION DATE	DELIVERY MODE
03/21/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/542,833	VAN SCHAIJK ET AL.	
	Examiner	Art Unit	
	EVAN PERT	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,9 and 12-15* is/are rejected.

7)☒ Claim(s) *2-8,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *0705*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to for the following informalities:

- At page 2, line 11, “if the” should read –is the--.
- At page 3, line 27, “technology node” should seemingly read --state of the art—or –technology mode--, or an equivalent since “technology node” is not readily understood.
- At page 6, line 17, “drawn on scale” should read –drawn to scale--.
- At page 7, first line, --and—should be inserted before “silicon-on sapphire."

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 13 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention:

The term "sub-lithographically dimensioned slit" in claim 13 is a relative term which renders the claim indefinite. As explained by applicant and as is known in the art, the actual “dimension” being claimed (i.e. distance between floating gates in the word line direction) is “dependent on [evolving] technology and on process conditions" [applicant’s specification, page 3, lines 26-29]:

Since the dimensional limit of lithography changes with time as state-of-the-art advances, the dimension being claimed is indefinite, dependent on the date at which the claim is enforced, the dimension shrinking as advances continue in the art.

Therefore, any slit with a very small dimension compared to the earliest photolithography limits can reasonably be considered to be indistinguishable from a "sub-lithographically dimensioned slit."

For purposes of examination, the term “sub-lithographically dimensioned slit” is considered to be ambiguous, and thus bears insignificant patentable weight as to the actual definite "dimension" of the claimed slit.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,261,905 [IDS #0705].

Notably, applicant’s specification and pending claims do not limit the term “floating gate separator” to separate only in the word line direction, so the act of separation of floating gates in the bit line direction by nitride strips 440 makes it reasonable to call the strip 440 in the ‘905 reference a “floating gate separator.”

Regarding claims 1 and 9, the '905 reference discloses a method for manufacturing an array of semiconductor devices on a substrate [i.e. an "EPROM"], each device having a floating gate [e.g. 450 in Fig. 4c], comprising: first forming isolation zones [e.g. 410 in Fig. 4a] in the substrate, thereafter forming a floating gate separator made of nitride [e.g. 440] on the isolation zones at locations where separations between adjacent floating gates are to be formed [i.e. the floating gate separator strips 440 separate floating gates in the bit line direction], after forming the floating gate separator, forming the floating gates on the substrate between parts of the floating gate separator [i.e. forming floating gates 450 on the substrate between parts of floating gate separator 440], and thereafter removing the floating gate separator [col. 8, lines 16-18] so as to obtain slits in between neighboring floating gates [as seen in Fig. 4c, when the floating gate separator strips 440 are removed there is a gap [or as deemed by applicant, "a slit," between adjacent floating gates 450 in the bit line direction].

5. Claims 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Sandhu et al. (US 6,614,072) in view of Watanabe et al. (US 5,889,304).

The '304 reference is relied on as secondary reference in a 102 rejection for teaching a universal fact that the floating gates in Fig. 1 of the '072 reference each inherently have "a sharp tip of floating gate material" in both directions of the word line [see Fig. 1 of the '072 reference taken with its col. 16, lines 38-50].

Regarding claim 12, the '702 reference discloses an array of semiconductor devices with a floating-gate to control-gate coupling ratio [Fig. 1], comprising: a substrate with a planar surface [24 wherein the substrate is a flat surface substrate seen along the bit line edge of the drawing], an isolation zone in the substrate in the planar surface [26 wherein claim 12 does not state that the isolation region must be planar with the flat surface of the substrate as applicant's specification indicates that "LOCOS can be used" per page 7, lines 9-13], at least two floating gates [30] extending on the substrate in a first direction [i.e. in the "word line direction"], each floating gate partially overlapping the isolation zone [i.e. 30 overlaps 26 as seen in Fig. 1] and comprising floating gate material [wherein 30 is inherently a "floating gate material" because the material is a "floating gate"], a slit between the two floating gates [i.e. a gap where control gate 34 and dielectric 32 drop in and divide the floating gates 30 in the word line direction], and a control gate [34] extending laterally with respect to the planar surface over the floating gates [seen in Fig. 1], wherein at least one of the floating gates is provided with a sharp tip of floating gate material both in the first direction and in a second direction including an angle with the first direction [i.e. the two ends of each floating gate in the word line direction have sharp tips because the tips are on a slant of LOCOS oxide 26 and this cause the angle to be less than 90°, as explained by the '072 reference [see Fig. 1 of the '072 reference taken with its col. 16, lines 38-50].

Regarding claim 13, the dimension of the slit (i.e. the dimension of the gap between floating gate 30 where control gate 34 and dielectric 32 separate floating gates 30) is very small in the '072 reference, so the "sub-lithographically dimensioned" limitation of claim 13 is not considered as having significant patentable weight, in view of the rejection under 35 USC 112, 2nd above.

Regarding claims 14 and 15, “a flat top surface” (i.e. a flat top surface is over the flat part of the substrate between isolation regions 26), wherein claim 14 does not require the “entire top surface” to be flat.

Allowable Subject Matter

6. Claims 2-8 and 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Notably, while the European Search Report implies that references (cited on IDS #0705) disclose the limitations of claims 10 and 11, these references actually do not at all suggest or disclose a floating gate separator “comprising at least two layers of different material” or a step that includes “forming spacers on the floating gate separator before forming the floating gates.”

Furthermore, it should be noted that device claims could be distinguished from prior art if the claimed “isolation zone in the substrate in the planar surface” were additionally limited to be “planar with the planar surface of the substrate.”

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US 6,573,139; US 6,309,926; and US 5,566,106 are cited for disclosing NVM devices wherein the slit dimension between floating gates in the word line direction is a particular focus of discussion.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to EVAN PERT whose telephone number is (571)272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ETP
March 14, 2008

/Evan Pert/
Primary Examiner, Art Unit 2826